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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/987,914	11/16/2001	Takayuki Oshima	HITA-0120	7936

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EXAMINER	
BREWSTER, WILLIAM M	
ART UNIT	PAPER NUMBER
2823	8

DATE MAILED: 04/02/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Application N .	Applicant(s)	
	09/987,914	OSHIMA ET AL.	
	Examiner	Art Unit	
	William M. Brewster	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 March 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) *1-17 and 28-37* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *18-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

Claims 1-17 withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in Paper No. 5.

Claims 28-37 withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected species, there being no allowable generic or linking claim. Election was made **without** traverse in Paper No. 7.

Applicant's election without traverse of claims 18-27 in Paper No. 7 is acknowledged.

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 18, 19, 21, 23, 24, 25 are rejected under 35 U.S.C. 102(b) as being anticipated by Tadashi, Japanese Publication No. 11-111,845.

Tadashi anticipates a method of fabricating a semiconductor device having wirings formed in wiring grooves and a connection member formed integrally with the wirings in via holes for connecting the wirings and lower layer wirings thereof comprising the steps of: (a) in fig. 3B, forming a first dielectric layer 31 having a relatively small Young's modulus, less than 60 GPa, SiOF and, in fig. 3d, a second dielectric layer, SiO_2, having a relatively large Young's modulus, 60 GPa or more, successively on a

substrate, (b) in fig. 3E, forming the via holes at predetermined regions of the first dielectric layer and forming the wiring grooves at predetermined regions, within 41, of the second dielectric layer, and (c) burying a conductive member 41 inside the via holes and the wiring grooves, wherein the specific dielectric constant of the first dielectric layer is less than the specific dielectric constant of the second dielectric layer; in fig. 3D, wherein a stopper dielectric film 32, comprising SiN, of a relatively thin film thickness is formed to an upper layer of the first dielectric layer in the step (a); wherein the first dielectric layer and the second dielectric layer are formed by a CVD method, p. 4, ¶ 24-33.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 20, 22, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tadashi in view of Wolf.

Tadashi teaches a method of fabricating a semiconductor device having wirings formed in wiring grooves and a connection member formed integrally with the wirings in via holes for connecting the wirings and lower layer wirings thereof comprising the steps of: (a) in fig. 3B, forming a first dielectric layer 31 having a relatively small Young's modulus, less than 60 GPa, SiOF and, in fig. 3d, a second dielectric layer, SiO_2, having

a relatively large Young's modulus, 60 GPa or more, successively on a substrate, (b) in fig. 3E, forming the via holes at predetermined regions of the first dielectric layer and forming the wiring grooves at predetermined regions, within 41, of the second dielectric layer, and (c) burying a conductive member 41 inside the via holes and the wiring grooves, wherein the specific dielectric constant of the first dielectric layer is less than the specific dielectric constant of the second dielectric layer; in fig. 3D, wherein a stopper dielectric film 32, comprising SiN, of a relatively thin film thickness is formed to an upper layer of the first dielectric layer in the step (a); wherein the first dielectric layer and the second dielectric layer are formed by a CVD method, p. 4, ¶ 24-33.

Tadashi does not specify the main conductive layer to be copper, but Wolf, V. II, pp. 192-4. Tadashi states and gives motivation for using copper, wherein a main conductive layer buried inside the via holes and the wiring grooves comprises copper, on p. 193, ¶ 2. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that combining Wolf's process with Tadashi's invention would have been beneficial because low resistivity and good electromigration resistance.

Neither Tadashi nor Wolf specify the hole diameter of the via hole is about 0.5 μms, but this dimension may be optimized.

"Normally, it is to be expected that a change in temperature, or in concentration, or in both, would be an unpatentable modification. Under some circumstances, however, changes such as these may impart patentablility to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not

merely degree from the results of the prior art . . . such ranges are termed 'critical ranges' and the applicant has the burden of proving such criticality . . . More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation."

In re Aller 105 USPQ 233, 255 (CCPA 1955). See also In re Waite 77 USPQ 586 (CCPA 1948); In re Scherl 70 USPQ 204 (CCPA 1946); In re Irmscher 66 USPQ 314 (CCPA 1945); In re Norman 66 USPQ 308 (CCPA 1945); In re Swenson 56 USPQ 372 (CCPA 1942); In re Sola 25 USPQ 433 (CCPA 1935); In re Dreyfus 24 USPQ 52 (CCPA 1934).

Note that the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising there from. Where patentability is aid to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William M. Brewster whose telephone number is 703-305-5906. The examiner can normally be reached on Full Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 703-306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are 703-305-3432 for regular communications and 703-305-3432 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

WB
March 31, 2003

Olik Chaudhuri
Supervisory Patent Examiner
Technology Center 2800